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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,066	02/12/2002	Suzette K. Pangrle	50432-104	2391

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EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,066	PANGRLE ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cov r sh et with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8, 10-17* is/are pending in the application.

4a) Of the above claim(s) *16 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/12/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-8, 10-15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-8, 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami (U.S. Patent No. 6,133,137) in view of the Mikagi (U.S. Patent No. 6,153,507), previously applied.

Usami teaches in figures 2, 3A-3F a method of forming a composite dielectric on a substrate, the method comprising:

Forming a low dielectric constant (low-k) dielectric layer (204, called "insulating layer" in Usami, see col. 4, lines 42-45) by spin-on-glass techniques (SOG/HSQ, see figure 3b, col. 4, lines 42-45 and col. 2, lines 19-20),

HSQ is a low-k dielectric layer (see col. 1, lines 20-28),

The dielectric layer (204) formed from a silsesquioxane dielectric material or derivative thereof (HSQ, see col. 4, lines 42-45 and col. 1, lines 24-29 and figure 3B),

Forming a patterned photoresist (206, see figure 3C, col. 4, lines 57-61) on the dielectric layer (204),

Etching through the dielectric layer (204) to expose surface therein (surface inside through hole 207, see figure 3D, col. 4, lines 64-67, meeting claims 1, 6 and 9), and

Treating the exposed surface of the dielectric layer (204/209, see figure 3F,) with phosphine gas or plasma (col. 5, lines 34-41 and claim 1 of Usami, meeting claims 1, 7 and 9), and

Forming a cap layer (107, see figure 2, col. 4, lines 16-18) directly on the treated surface (106/209) of the dielectric layer (204, meeting claim 1).

Regarding to claim 2, forming the dielectric layer (204) by spin-on-glass techniques (SOG, see figure 3b, col. 4, lines 42-45 and col. 2, lines 19-20).

Regarding to claim 8, forming the dielectric layer (204) from a silsesquioxane dielectric material or derivative thereof (HSQ, see col. 4, lines 42-45 and col. 1, lines 24-29 and figure 3B).

Regarding to claim 10, removing the photoresist layer (206, see figure 3E, col. 5, lines 3-4), and

Forming a conformal barrier layer (see col. 4, lines 17-19 and figure 2, not shown) on the dielectric layer (204, inside the through hole 207, see figures 2 and 3F) including the phosphine plasma treated side surfaces thereof (106/209, see figures 2 and 3F and col. 5, lines 34-41).

Regarding to claim 11, forming a conductive layer (107) comprising copper (107, see figure 2, col. 4, lines 16-19) on the conformal barrier layer (see figure 2, col. 4, lines 17-19) and within the etched dielectric layer (204, see figures 2 and 3F, col. 4, lines 16-19).

Regarding to claim 12, polishing the conductive layer (see figure 2, col. 3, lines 65-68) to the barrier layer (see figure 2, col. 4, lines 17-19) to form a conductive trench or plug (107, see figure 2, col. 4, lines 16-19) within the dielectric layer (204).

Regarding to claim 13, forming a cap layer (108, see figure 2) over the conductive layer (107) and barrier layer (see col. 4, lines 17-19, not shown in figure 2).

Regarding to claim 14, the dielectric layer (204) comprises a porous silicon oxide (see figure 3B, col. 4, lines 42-45 and col. 1, lines 26-28).

Regarding to claim 15, depositing the silicon oxide (204) at a thickness of about 0.3 microns to about 1 micron (4000 A° or 0.4 microns, see col. 4, lines 40-41).

Usami teaches forming a composite dielectric layer on a substrate, using an ECR plasma chamber to generate plasma (see col. 5, lines 13-15) and forming a cap layer as described above. However, Usami does not teach using a semiconductor substrate (as claimed in claims 1), introducing the substrate to a PECVD chamber, introducing phosphine together with a carrier gas to the PECVD chamber as the phosphine source, cap layer is a dielectric and formed in-situ after treating the exposed surface of the dielectric layer (as claimed in claims 1, 3-4). Nevertheless, using a semiconductor substrate, introducing the substrate to a PECVD chamber, introducing phosphine together with a carrier gas to the PECVD chamber as the phosphine source, forming the cap layer by PECVD is a dielectric and formed in-situ after treating the exposed surface of the dielectric layer are known in semiconductor processing art as evidenced by Mikagi. Mikagi

teaches using a semiconductor substrate (101, a silicon, see figure 6A, col. 7, lines 34-35) (meeting claims 1 and 9), introducing the substrate to a PECVD chamber and PECVD is a ECR plasma chamber (see col. 8, lines 25-29) (meeting claim 3), introducing phosphine (see col. 8, lines 33-36) together with a carrier gas (nitrogen, an inert gas, in Mikagi, see col. 8, lines 58-61) to the PECVD chamber as the phosphine source (see col. 8, lines 33-45, meeting claim 4), forming the cap layer of any insulating layer (110a, see col. 8, lines 62-67) by PECVD is a dielectric and formed in-situ after treating the exposed surface of the dielectric layer (see col. 8, lines 56-67, meeting in claim 1)(Noted that since both cap layer and treating the exposed surface of the dielectric layer in the same vacuum apparatus of PECVD chamber, hence, cap layer deposition is an in-situ process).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time the invention was made would use a semiconductor substrate to form a semiconductor device and recognize that ECR plasma chamber is a PECVD chamber for forming a composite dielectric on a semiconductor substrate, introducing the substrate to a PECVD chamber, introducing phosphine together with a carrier gas to the PECVD chamber as the phosphine source, forming the cap layer by PECVD is a dielectric and formed in-situ after treating the exposed surface of the dielectric layer in the process of Usami as taught by Mikagi ***because*** semiconductor device can be formed directly on the semiconductor substrate without the need of forming an epitaxial semiconductor layer on the substrate that is not a semiconductor substrate, and PECVD chamber generates high density plasma for forming highly uniform dielectric layer, and the surface of dielectric layer treated with phosphine gas or plasma increases adhesion and preventing moisture in the copper via plug.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Usami (U.S. Patent No. 6,133,137) in view of the Mikagi (U.S. Patent No. 6,153,507) as applied to claims 1-4, 6-8, 10-15 above, and further in view of Shin et al (U.S. Patent No. 6,376,876), newly cited.

Usami teaches forming a composite dielectric layer on a substrate, using an ECR plasma chamber to generate plasma (see col. 5, lines 13-15) and forming a cap layer as described above. However, Usami does not teach forming a cap layer is selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide and composites thereof. Nevertheless, using a semiconductor substrate, forming a cap layer is selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide and composites thereof are known in semiconductor processing art as evidenced by Shin et al.. Shin et al. teaches using a semiconductor substrate (20), forming a cap layer (32) is selected from the group consisting of silicon nitride, silicon oxynitride, or silicon oxide (see figure 5b, col. 8, lines 45-50).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time the invention was made would use a semiconductor substrate to form a semiconductor device and recognize that forming a cap layer by using either silicon nitride, silicon oxynitride, or silicon oxide in process of Usami as taught by Shin et al. because forming a cap layer using either silicon nitride, silicon oxynitride, or silicon oxide would protect the underlayer.

Response to Arguments

Applicant's arguments with respect to claims 1-8, 10-15 have been considered but are moot in view of the new ground(s) of rejection.

The objection of the specification is overcome by the amendment.

Applicants contend that Usami does not teach or suggest treating the surface of a dielectric layer with phosphine and/or phosphine plasma and forming a cap layer directly on the treated surface of the dielectric layer and dielectric layer is a low-k dielectric material in the newly amended claim 1. This is not found to be persuasive because Usami clearly teaches treating the surface of a dielectric layer (209/204, see figure 3F, col. 5, lines 34-41 and claim 1 of Usami) with phosphine and/or phosphine plasma (PH_3) and forming a cap layer (107, see figure 2, col. 4, lines 16-18) directly on the treated surface of the dielectric layer (106/209/204). And, Usami teaches dielectric layer (204) is a low dielectric constant material of HSQ material (see col. 4, lines 40-46 and col. 1, lines 19-33).

Applicants also contend that Usami shows the opposite by treating the side surface of via hole and then fills the via with a conductive material rather than forming a cap dielectric layer. This is not found to be persuasive because there is not seen that the claimed limitation of the treating expose surface of dielectric layer as claimed in claim 1 precludes the treating exposed side surface of dielectric layer. Usami clearly shows that using phosphine plasma (PH_3) treats the exposed surface in the via hole (207) of dielectric layer (106/209) and a cap layer (107) directly formed on the treated dielectric layer (106/209, see figures 2 and 3F, col. 5, lines 34-41). Therefore, the treated exposed side surface of the dielectric layer in via hole clearly meets the claimed limitation of the treating exposed surface of dielectric layer as claimed in claim 1.

Applicants contend that Usami does not teach the cap layer is a dielectric layer. This is not found to be persuasive because the secondary reference Mikagi clearly teaches that a cap layer can be a dielectric layer (110a, see fig. 7F and col. 8, lines 62-67) formed on the phosphine

plasma (PH_3) treated surface (104b/108a). Since, Mikagi teaches forming a dielectric layer on the phosphine plasma (PH_3) treated surface, hence, it would have been obvious to a person of ordinary skill in the art at the time the invention to form a dielectric cap layer on the phosphine plasma treated surface in the Usami's process because the cap layer prevents the impurities from migrating into the dielectric layer.

Applicant also contends that Usami does not teach or suggest the step of forming a cap layer in-situ in the newly amended claim 1. Applicants also contend that Mikagi does not describe forming a cap layer, in-situ, after treating the exposed surface of the dielectric layer in the newly amended claim 1. This is not found to be persuasive because the secondary reference Mikagi teaches using PECVD reactor to form dielectric layer (104b) and cap layer (110a) and treating dielectric layer (104b) in a vacuum apparatus. Since, PECVD reactor is a vacuum apparatus, hence, it is obvious to an ordinary skill in the art that the cap layer (110a) is formed in the same (in-situ) PECVD reactor after treating the dielectric layer (104b) (see col. 8, lines 56-67). Therefore, it would have been obvious to an ordinary skill in the art to modify Usami's process with same PECVD reactor to form a cap layer on the dielectric layer and treating the dielectric layer with a phosphine plasma (PH_3) because using the same PECVD reactor that is a vacuum apparatus to form plasma gas for both depositing and treating process can lower the processing cost.

Applicant contends that Mikagi using similar processes in forming various dielectric layers which does not equate to the step of in-situ process. This is not found to be persuasive because Mikagi teaches forming a dielectric layer (104b) in a PECVD chamber (see col. 8, lines 25-32), treating the exposed surface of the dielectric layer (104b) by introducing phosphine in a

vacuum apparatus (see col. 8, lines 33-55), then forming a cap layer (110a) with a PECVD chamber (see col. 8, lines 63-65). Since, PECVD reactor is a vacuum apparatus, hence, it is obvious to an ordinary skill in the art that the cap layer (110a) is formed in the same (in-situ) PECVD reactor after treating the dielectric layer (104b) (see col. 8, lines 56-67). Therefore, it would have been obvious to an ordinary skill in the art to modify Usami's process with same PECVD reactor to form a cap layer on the dielectric layer and treating the dielectric layer with a phosphine plasma (PH_3) because using the same PECVD reactor that is a vacuum apparatus to form plasma gas for both depositing and treating process can lower the processing cost.

From above, the examiner has shown that combination of Usami in view of Mikagi with proper motivation as set forth in the last office action, hence, the combination of claims 1-4, 6-8, 10-15 is not allowable under 35 USC 103(a) that would have been obvious to a person of ordinary skill in the art because Usami in view of Mikagi teaches forming a cap dielectric layer directly on the treated surface of the dielectric layer, and forming cap dielectric layer, dielectric layer and treating the exposed surface of the dielectric layer in the same (in-situ) vacuum apparatus to lower the process cost and preventing impurities from migrating into the dielectric layer.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (703) 308-9439, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:30AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (703) 308-4940. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN
6/25/03